# ----------------------------------------------------------------------

# Name Type Size Value

# ----------------------------------------------------------------------

# uvm\_test\_top edgedetect\_uvm\_test - @360

# env edgedetect\_uvm\_env - @372

# agent edgedetect\_uvm\_agent - @380

# agent\_ap\_compare uvm\_analysis\_port - @414

# agent\_ap\_output uvm\_analysis\_port - @405

# drvr edgedetect\_uvm\_driver - @546

# rsp\_port uvm\_analysis\_port - @563

# seq\_item\_port uvm\_seq\_item\_pull\_port - @554

# mon\_cmp edgedetect\_uvm\_monitor\_compare - @580

# mon\_ap\_compare uvm\_analysis\_port - @590

# mon\_out edgedetect\_uvm\_monitor\_output - @572

# mon\_ap\_output uvm\_analysis\_port - @604

# seqr uvm\_sequencer - @423

# rsp\_export uvm\_analysis\_export - @431

# seq\_item\_export uvm\_seq\_item\_pull\_imp - @537

# arbitration\_queue array 0 -

# lock\_queue array 0 -

# num\_last\_reqs integral 32 'd1

# num\_last\_rsps integral 32 'd1

# sb edgedetect\_uvm\_scoreboard - @388

# compare\_fifo uvm\_tlm\_analysis\_fifo #(T) - @689

# analysis\_export uvm\_analysis\_imp - @733

# get\_ap uvm\_analysis\_port - @724

# get\_peek\_export uvm\_get\_peek\_imp - @706

# put\_ap uvm\_analysis\_port - @715

# put\_export uvm\_put\_imp - @697

# output\_fifo uvm\_tlm\_analysis\_fifo #(T) - @636

# analysis\_export uvm\_analysis\_imp - @680

# get\_ap uvm\_analysis\_port - @671

# get\_peek\_export uvm\_get\_peek\_imp - @653

# put\_ap uvm\_analysis\_port - @662

# put\_export uvm\_put\_imp - @644

# sb\_export\_compare uvm\_analysis\_export - @627

# sb\_export\_output uvm\_analysis\_export - @618

# ----------------------------------------------------------------------

#

# UVM\_INFO ../uvm/edgedetect\_uvm\_sequence.sv(30) @ 0: uvm\_test\_top.env.agent.seqr@@seq [SEQ\_RUN] Loading file ../images/copper\_720\_540.bmp...

# UVM\_INFO ../uvm/edgedetect\_uvm\_sequence.sv(53) @ 7775865: uvm\_test\_top.env.agent.seqr@@seq [SEQ\_RUN] Closing file ../images/copper\_720\_540.bmp...

# UVM\_INFO /vol/mentor/questa\_sim-2019.3\_2/questasim/verilog\_src/uvm-1.2/src/base/uvm\_objection.svh(1270) @ 7790715: reporter [TEST\_DONE] 'run' phase is ready to proceed to the 'extract' phase

# UVM\_INFO ../uvm/edgedetect\_uvm\_monitor.sv(141) @ 7790715: uvm\_test\_top.env.agent.mon\_cmp [MON\_CMP\_FINAL] Closing file ../images/copper\_sobel.bmp...

# UVM\_INFO ../uvm/edgedetect\_uvm\_monitor.sv(69) @ 7790715: uvm\_test\_top.env.agent.mon\_out [MON\_OUT\_FINAL] Closing file ../images/output.bmp...

# UVM\_INFO /vol/mentor/questa\_sim-2019.3\_2/questasim/verilog\_src/uvm-1.2/src/base/uvm\_report\_server.svh(847) @ 7790715: reporter [UVM/REPORT/SERVER]

# --- UVM Report Summary ---

#

# \*\* Report counts by severity

# UVM\_INFO : 10

# UVM\_WARNING : 0

# UVM\_ERROR : 0

# UVM\_FATAL : 0

# \*\* Report counts by id

# [MON\_CMP\_FINAL] 1

# [MON\_OUT\_FINAL] 1

# [Questa UVM] 2

# [RNTST] 1

# [SEQ\_RUN] 2

# [TEST\_DONE] 1

# [UVM/RELNOTES] 1

# [UVMTOP] 1

#

# \*\* Note: $finish : /vol/mentor/questa\_sim-2019.3\_2/questasim/verilog\_src/uvm-1.2/src/base/uvm\_root.svh(517)

# Time: 7790715 ns Iteration: 70 Instance: /edgedetect\_uvm\_tb

# End time: 22:15:43 on Feb 05,2024, Elapsed time: 0:00:24

# Errors: 0, Warnings: 0

Simulation Cycle Count = **779,071 cycles**

Time Complexity = O(2N) == **O(N)**

FIFO Buffer Size = **8**

FPS = **128 FPS** (1 frame / 7790715 ns or 0.007790715 s)

LUTs for combinational functions (total\_luts): 638

I/O Pins: 38

DSP Blocks (dsp\_used): 1(15)

Non I/O registers (non\_io\_reg): 534

I/O Registers (total\_io\_reg): 0

Memory Bits: 11456

Max Frequency for Design: **92.4 MHz**

More resource utilization details:

Total combinational functions 638 of 6272 (10%)

Logic element usage by number of inputs

4 input functions 170

3 input functions 140

[=2 input functions 328

Logic elements by mode

normal mode 363

arithmetic mode 275

Total registers 534 of 6272 ( 8%)

I/O pins 38 of 180 (21%), total I/O based on largest package of this part.

Number of I/O registers

Input DDRs :0

Output DDRs :0

DSP.Simple\_Multipliers\_18\_bit: 1

DSP Blocks: 1 (2 nine-bit DSP elements).

DSP Utilization: 6.67% of available 15 blocks (30 nine-bit).

ShiftTap: 0 (0 registers)

Ena: 451

Sload: 64

Sclr: 26

Total ESB: 11456 bits

edgedetect\_top:

A diagram of a computer

Description automatically generated

sobel:

A blueprint with green lines and squares

Description automatically generated

Shift Register:

A diagram of a computer

Description automatically generated